PCI 9080-3 Data Book Addendum

A. Affected Silicon Revision

This document details addendum documentation for the following silicon:

Product	Revision	Description	Status
PCI 9080	9080-3	PCI I/O Accelerator	Production

B. Documentation Version

The following documentation details the silicon baseline functional description:

Document	Version	Description	Publication Date
PCI 9080 Data Book	1.06	Data Book	January 2000

C. Addendum Documentation Revision History

Revision	Date	Description
1.0	6/3/05	*PCI 9080 Data Book* additions and corrections; including lead-free model numbers.

D. Addendum Documentation Summary

#	Description
1	PCI 9080 Lead-Free ROHS-Compliant Versions
2	Differences between the PCI 9060SD and PCI 9080
3	Delayed Read Retry/Disconnect
4	DMA Abort
5	DMA Threshold Register (DMATHR; PCI:B0h, LOC:130h) Maximum Values
6	Internal Pull-Up and Pull-Down Resistors
7	Power Supply to PCI I/O Buffers on a Universal Add-in Card
8	Serial EEPROM Chip Select (EECS) Timing
9	Thermal Resistance
10	Local Bus Input Pin Minimum Setup and Hold Times, and Output Pin Maximum Output Delay Specifications

1. PCI 9080 Lead-Free ROHS-Compliant Versions

The PCI 9080 is available in leaded packaging and lead-free ROHS packaging. Ordering information is delineated in the following table.

Part Number	Package
PCI 9080-3	Standard Leaded PQFP Package
PCI 9080-3 G	Lead-Free ROHS Green PQFP Packaging
PCI 9080-3HR	Leaded PQFP Package

2. Differences between the PCI 9060SD and PCI 9080

The PCI 9080 is upward compatible with the PCI 9060, PCI 9060ES and PCI 9060SD, except as noted in the *PCI 9080 Data Book*, v1.06, Section 1.4, "Compatibility of PCI 9080 with PCI 9060, PCI 9060ES and PCI 9060SD," and Section 4.1 "New Register Definitions Summary." There are additional differences between the PCI 9060SD and the PCI 9080 that are not specifically listed in these sections of the *PCI 9080 Data Book*, v1.06:

- The Extra Long Load of the serial EEPROM layout is different between the two devices. In the PCI 9080, the Subsystem and Subsystem Vendor IDs are at the top of that space, and all other values shift down two places. Therefore, the PCI 9060SD EEPROM image must be modified for use with the PCI 9080, if the Extra Long Load from EEPROM is enabled (by Local register PCI offset 18h, bit 25, being set to 1).
- If the Local Address Space 1 Range register (LAS1RR) is programmed to map address space to PCIBAR3, but the Space 1 Enable bit (LAS1BA[0]) is not set during initialization by the serial EEPROM or Local Bus CPU, the PCI 9080 does not request address space when the BIOS or OS tries to configure PCIBAR3 (reading PCIBAR3 after writing FFFFFFFFh returns 0h, rather than the Range register value). The PCI 9060SD returns the Range register value in such case, regardless of the LAS1BA[0] value. Accordingly, BIOS will normally allocate address space to PCIBAR3. Therefore, when replacing a PCI 9060SD with a PCI 9080, if Local Address Space 1 is used, LAS1BA[0] must be set during initialization (by the serial EEPROM or Local Bus CPU).
- The LAS1BA[0] description in the *PCI 9080 Data Book*, v1.06, Table 4-46, states that if this bit is not set, BIOS does not allocate address space PCIBAR3. This difference should also be documented as a separate line item in Table 4-4, "Register Differences between the PCI 9080 and PCI 9060SD."

3. Delayed Read Retry/Disconnect

The name for the Mode/DMA Arbitration register bit 24 (MARBR[24]) is changed from "PCI Specification v2.1 Mode" to "*PCI r2.1* Features Enable." The *PCI 9080 Data Book*, v1.06, MARBR[24] register bit description, and Section 3.6.2.1, are revised as follows:

Table 4-35. (MARBR; PCI:08h or ACh, LOC: 88h or 12Ch) Mode/Arbitration Register

Bit	3.1.1.1.1 Description	Read	Write	Value after Reset
24	***PCI r2.1* Features Enable.** When set to 1, the PCI 9080 performs all PCI Read and Write transactions in compliance with *PCI r2.1*. Setting this bit enables Delayed Reads, 2^{15} PCI Clock timeout on Retries, 16- and 8-clock PCI latency rules, and enables the option to select PCI Read No Write Mode (Retries for writes) (bit 25) and/or PCI Read with Write Flush Mode (bit 26). Refer to Section 3.6.2.1 for additional information. Value of 0 causes TRDY# to remain de-asserted on reads until Read data is available. If Read data is not available before the PCI Target Retry Delay Clocks Counter (LBRD0[31:28]) expires, a PCI Retry is issued.	Yes	Yes	0

The following text replaces a portion of PCI 9080 Data Book section 3.6.2.1, starting from the title and continuing through to the second bulleted item, "Write and flush pending delayed read."

3.6.2.1 PCI r2.1 Features Enable

The PCI 9080 can be programmed through the *PCI r2.1* Features Enable bit (MARBR[24]) to perform all PCI Read/Write transactions, in compliance to the *PCI r2.1*. The following PCI 9080 behavior occurs when MARBR[24]=1.

3.6.2.1.1 Direct Slave Delayed Read Mode

PCI Bus single-cycle aligned or unaligned 32-bit Direct Slave Read transactions always result in a 1-Lword single-cycle transfer on the Local Bus, with corresponding Local Address and Byte Enables (LBE[3:0]#) asserted to reflect the PCI Byte Enables (C/BE[3:0]#), unless the PCI Read No Flush Mode bit is enabled (MARBR[28]=1). This causes the PCI 9080 to Retry all PCI Bus Read requests that follow, until the original PCI Address and Byte Enables (C/BE[3:0]#) are matched.

3.6.2.1.2 2^{15} PCI Clock Timeout

If a PCI Master does not complete its originally requested Direct Slave Delayed Read transfer, the PCI 9080 flushes the Direct Slave Read FIFO after 2^{15} PCI clocks and grants an access to a new Direct Slave Read access. The PCI 9080 Retries all other Direct Slave Read accesses that occur before the 2^{15} PCI clock timeout.

3.6.2.1.3 *PCI r2.1* 16- and 8- Clock Rule

The PCI 9080 guarantees that if the first Direct Slave Write data cannot be accepted by the PCI 9080 and/or the first Direct Slave Read data cannot be returned by the PCI 9080 within 16 PCI clocks from the beginning of the Direct Slave cycle (FRAME# asserted), the PCI 9080 issues a Retry (STOP# asserted) to the PCI Bus.

During successful Direct Slave Read and/or Direct Slave Write accesses, the subsequent data after the first access is accepted for writes or returned for reads in 8 PCI clocks (TRDY# asserted). Otherwise, the PCI 9080 issues a PCI disconnect (STOP# asserted) to the PCI Master.

In addition, setting the *PCI r2.1* Features Enable bit (MARBR[24]=1) allows optional enabling of the following *PCI r2.1* function:

- No write while Delayed read is pending (PCI Retries for writes) (MARBR[25])

The following *PCI 2.1* optional function can be activated except if MARBR[25]=1, and should not be enabled if MARBR[24]=0:

- Write and flush pending Delayed read (MARBR[26])

4. DMA Abort

In the *PCI 9080 Data Book*, v1.06, Section 3.7.6.2, “DMA Abort,” which provides instructions to abort DMA under software control, replace step 5 which states:

“Abort DMA by programming the Channel Abort bit (DMACSR0[2] = 1)”,

with

“Abort DMA by programming the Channel Abort bit while keeping the Start bit set (DMACSR0[2:1]=11b (*that is*, write the value 6h to DMACSR0[7:0]).”

5. DMA Threshold Register (DMATHR; PCI:B0h, LOC:130h) Maximum Values

Replace the formulas provided in the DMA Thresholds register (DMATHR), and the note below Table 4-74, with the following note:

Note: *DMA Threshold register (DMATHR) maximum values for each of the 4-bit fields are calculated, according to the following formulas:*

- *For DMA Channel 0 (32-Lword FIFO), the threshold calculation is: AlmostFull + AlmostEmpty < 15*
- *For DMA Channel 1 (16-Lword FIFO), the threshold calculation is: Almost Full + AlmostEmpty <= 16*

6. Internal Pull-Up and Pull-Down Resistors

Update the Pin Summary, Section 5.1, to include the following details:

The *PCI 9080 Data Book*, v1.06, Section 5.1, "Pin Summary," incorrectly states that Local Bus internal pull-up resistors are 2K Ohms and that Local Bus internal pull-down resistors are 100K Ohms. All internal pull-up and pull-down resistors are valued at 50K Ohms nominal.

The EEDO pin requires an external pull-up resistor for reliable EEPROM access.

7. Power Supply to PCI I/O Buffers on a Universal Add-in Card

Add the following text to the VDDH (PCI) pin description in Table 5-2:

On Universal add-in card designs (in which the edge connector keying allows the card to be plugged into either 5V or 3.3V slots), connect the PCI 9080 VDDH (PCI) pins, which power the PCI I/O buffers, to the edge connector VIO pins (and not to the edge connector 5V or 3.3V pins). Also refer to the *PCI Local Bus Specification*, r2.1, Section 4.4.2.1, for VIO pin decoupling requirements.

8. Serial EEPROM Chip Select (EECS) Timing

Add the following text to the EECS pin description in Table 5-3:

To download serial EEPROM contents to registers, the PCI 9080 asserts EECS when it toggles the serial EEPROM clock EESK high.

9. Thermal Resistance

Add Thermal Resistance to Section 6, "Electrical Specifications":

Thermal Resistance is 30 to 50 °C/W.

10. Local Bus Input Pin Minimum Setup and Hold Times, and Output Pin Maximum Output Delay Specifications

Update Table 6-5 "AC Electrical Characteristics (Local Inputs) Estimated over Operating Range", and Table 6-6 "AC Electrical Characteristics (Local Outputs) Estimated over Operating Range," with the timing specifications shown in the tables below:

The PCI 9080 Local Bus Input pin minimum Setup and Hold times, and Output pin Maximum Output Delay times, are listed below.

Some of the input pin Hold time values differ from those listed in Table 6-5 of the *PCI 9080 Data Book*, v1.06 (and prior versions). Maximum Output Delay times for both ADS# and the Local Address outputs, listed below, differ from those listed in Table 6-6 of the *PCI 9080 Data Book*, v1.06 (and prior versions).

Timings that differ from the *PCI 9080 Data Book*, v1.06, are printed in **boldface and highlighted in yellow**.

Table 6-5. AC Electrical Characteristics (Local Inputs) Estimated over Operating Range

Signals (Synchronous Inputs) C_L = 50pF, V_{CC} = 5.0V 5%	T_{SETUP}(ns)	Old T_{HOLD} (ns)	New T_{HOLD} (ns)
ADS#	6	1	**2.01**
BIGEND#	4	0	0
BLAST#	6	0	0
BREQi	7	0	0
BTERM#	7	1	**1.5**
DP[3:0]	4	0	0
DREQ[1:0]#	3	1	**1.5**
EOT0#	7	1	**1.5**
EOT1#	1	1	**1.5**
LA[31:0]	5	0	0
LAD[31:0]	5	0	**1.69**
LBE[3:0]#	7	0	**1.25**
LD[31:0]	5	0	0
LHOLDA	7	2	**2.5**
LINTi	7	0	0
LLOCK	4	0	0
LW/R#	9	0	0
READYi#	8	1	**1.5**
S[2:0]	1	2	**2.5**
USERi	4	0	0
WAITi#	13	0	0

Table 6-6. AC Electrical Characteristics (Local Outputs) Estimated over Operating Range

Signals (Synchronous Outputs) V_{CC} = 5.0V 5%	Old Output T_{VALID} (Max)	New Output T_{VALID} (Max)
ADS#	14.5	**15.0**
BLAST#	16	16
BREQo	13	13
BTERMo#	15	15
DACK[1:0]#	14	14
DEN#	13	13
DMPAF#	17	17
DP[3:0]	20	20
DT/R#	14	14
LA[31:2] (C Mode)	15.8	**16.3**
LABS[3:1]	12	12
LAD[31:0] (Address, J Mode)	12.1	**12.6**
LAD[31:0] (Data, J Mode)	15	15
LD[31:0] (32- and 16-Bit, C Mode)	15	15
LD[31:0] (8-bit C Mode)	20	20
LBE[3:0]#	16	16
LDSHOLD	12	12
LHOLD	13	13
LINTo#	13	13
LLOCKo#	12	12
LSERR#	12	12
LW/R#	14	14
PCHK#	12	12
READYo#	14	14
USERo	11	11
WAITo#	18	18