Assuring Data Integrity in an Optically Isolated 3.3 V I2C Bus

White Paper

By He Junhua
Optical Communication Solutions Division,
Avago Technologies Limited

The inter-IC bus (I2C bus) is being used in an increasing number of applications, including consumer appliances, communications equipment, and industrial equipment. In practically all cases, low voltage optocouplers are used to provide galvanic isolation in the 3.3V I2C bus interface. In a minimum configuration, three high speed optocouplers are used to isolate the CLK, SDA_in and SDA_out bus signals.

This article discusses how the parameters related to optocoupler propagation delay can affect data integrity and system reliability for applications requiring isolation of the I2C bus interface, including IEEE 802.3af-compliant power-over-Ethernet switches and the analog-to-digital conversion interface to microcontrollers. As examples, we are using Avago Technologies' HCPL-063L dual-channel and HCPL-060L single-channel 15 MBd 3.3 V optocouplers.

I2C Bus Basics

The I2C bus is a serial digital signal communication protocol developed by Philips Semiconductors. It requires only two wires and minimal hardware in the interface port, with interconnected devices addressed through software. Data speed between the master and slave devices ranges from the Standard Mode at 100 kb/s, through Fast Mode at 400 kb/s, to High Speed Mode at 3.4 Mb/s. The two wires carry SDA data and SCL clocking, with every one data bit of SDA being read at each SCL clock high period. The data must remain stable during this period. The high-to-low or low-to-high state transition can only be completed when the clock signal on the SCL line is low (Figure 1).

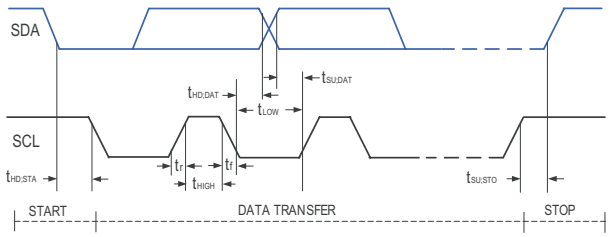

Figure 1. Timing Diagram of I2C Bus

Optocoupler Propagation Delay in the I2C Bus

Galvanic isolation in the I2C bus interface is required by the application environment to ensure error-free data transmission and isolate high voltage devices. Suitable optocouplers can provide this isolation.

High speed optocouplers, ranging from 100 kilobaud (kBd) to 50 megabaud (MBd), are available for digital data interface isolation. The appropriate optocoupler for the I2C bus interface primarily depends on the application's speed and propagation delay requirements.

First, an optocoupler's maximum high-to-low and low-to-high propagation delay, (tPHL and tPLH), will indicate the device's maximum data transmission rate (Figure 2a). The maximum propagation delay tP(MAX) is the greater of tPHL or tPLH. An optocoupler transmitting NRZ (non-return-to-zero) data requires that the data bit period t is at least greater than tP(MAX): $\tau \geq tP\ (MAX)$

So, the maximum data speed is: $FNRZ\ (MAX) = 1/\tau \leq 1/tP(MAX)$

For a clock signal which is RZ (return-to-zero) data, such as the I2C bus SCL, a clock cycle includes both the high and low period: $\tau = tHIGH + tLOW$

For a normal 50-percent duty cycle RZ clock signal, a safe rule in judging the expected RZ data rate is: $fRZ(MAX) \leq 1/2\ (tP(MAX))$

However, in the I2C bus clock cycle, the high period is permitted to be shorter than the low period. To transmit a less than 50 percent duty cycle signal over the optocoupler, the optocoupler's maximum propagation delay tP(MAX) should be less than the high period: $tHIGH \geq tP(MAX)$

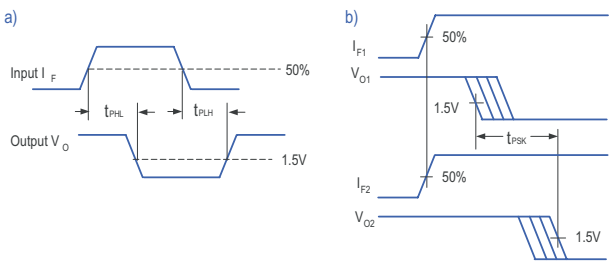

Figure 2. Optocoupler Propagation Delay and Skew

For example, when considering isolating an I2C bus at the Fast Mode clock frequency of 400 kHz and 50-percent duty cycle, which is equivalent to a 800 kBd data rate, the maximum propagation delay of the optocoupler can't exceed 1.25 µs. Since the I2C bus specification allows a Fast Mode clock hightime of as short as 0.6 µs, the optocoupler maximum propagation delay tP(MAX) must be shorter than 0.6 µs instead of 1.25 µs.

In high speed optocouplers the pulse width distortion (PWD) parameter is specified as the difference between tPHL and tPLH. Typically, PWD on the order of 20 percent to 30 percent of the minimum pulse width is tolerable.

When data is transmitted synchronously over parallel signal lines, the optocoupler's propagation delay skew tPSK is an important factor that may determine the maximum parallel data transmission rate. If the parallel data is being sent through two individual optocouplers or a single multi-channel optocoupler, differences in the propagation delays between channels will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delay is large enough, it will limit the maximum rate at which parallel data can be sent through the optocouplers.

As shown in Figure 2b, propagation delay skew is defined as the difference between the minimum and maximum propagation delays of tPLH and/or tPHL for any group of optocoupler channels operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). The tPSK of the optocouplers will result in uncertainty in both data and signal lines. In general, the absolute minimum pulse width that can be sent through parallel optocouplers is twice tPSK. A conservative design should use a slightly longer pulse width to ensure that any additional uncertainties caused elsewhere in the circuit do not cause problems. The I2C bus clock signal high period is the shortest pulse, so twice the optocoupler's propagation delay skew should not exceed the I2C clock high period.

The I2C bus protocol is level sensitive for the SCL and SDA signals. SDA should be stable at either the high or low level during the SCL high period. An I2C bus device must internally provide a data hold time tHD;DAT to bridge the undefined period between high and low levels of the falling edge of the SCL signal. Since an optocoupler will create uncertainty in both the SDA and SCL signals, data hold time tHD;DAT should be set greater than tPSK. The value of tPSK should also be considered in the SDA data set up time tSU;DAT.

The I2C bus protocol also requires that the output stages of transmitter devices connected to the bus must be open-drain or open-collector to perform the wired-AND function. Avago Technologies' HCPL-063L optocoupler has an open-collector output. With a tP(MAX) of 90 ns, this optocoupler is capable of transmitting high speed data. Its maximum propagation delay skew, tPSK, is as low as 40 ns which provides sufficient time to permit the I2C bus data hold/set up time.

Isolated Swap Controller in POE

An emerging industry standard, IEEE 802.3af, enables distributing power over an Ethernet cable. This network continues the same architecture as IEEE 802.3 Ethernet, but provides that either a spare pair or a signal pair of wires in the cable can carry -48 VDC to supply powered devices (PDs) such as IP phones, web cameras, and wireless LAN access points. Power sourcing equipment (PSE) is used to provide -48 VDC at the switch or hub.

802.3af-compliant PSE may be connected in two locations with respect to the link segment. The midspan connection implements the PSE technology outside an existing Ethernet switch. The endspan (or Endpoint/DTE PSE) connection implements the PSE inside the switch itself. So far, the majority of vendors have selected midspan PSE, although some have already integrated endspan PSE in their switches.

A PSE not only distributes power into the Ethernet network, but also provides a power management function. The power management function searches the link segment for a PD, classifies the power rating of the PD, supplies power to the link segment if a PD is detected, monitors the current on the link segment, and removes power from the link segment when the PD is disconnected or no longer requests power.

The 802.3af specification requires electrical isolation of both the PSE and PD, consistent with the requirements of the physical layers (PHYs) of 10/100BASE-T Ethernet. As mentioned previously, the PSE hot swap controller works with a –48 V power supply, which is connected to either a spare pair or the signal pair of wires in the LAN data cable. Electrical isolation is required between the hot swap controller and its host control circuit.

As shown in Figure 3, PSE hot swap controllers or power management chips incorporate I2C bus protocol to communicate with a host microcontroller. In this example, two HCPL-063L dual-channel 3.3 V optocouplers isolate the I2C bus interface between the hot swap controller chip and host microcontroller. The two channels of one HCPL-063L transmit clock and SDA_IN data from the host controller/master device to the hot swap controller/slave device. One channel of another HCPL-063L transmits SDA_OUT data from slave to master in a reversed direction. The second channel can interface with additional functions, such as port request/interrupt signals. A conservative design for the LED input resistor calls for a threshold current greater than 5 mA. A resistor of less than 200 Ω is recommended to limit the LED drive current to no greater than 7.5 mA. The two 3.3 V power supplies must be isolated between the host controller and hot swap controller.

The Avago Technologies' HCPL-063L is specified with an isolation voltage of 3750 Vrms for one minute (per UL1577), which will enable a POE switch to meet telecommunications equipment safety standards such as IEC 60950. The 15 kV/µs common-mode transient immunity of the HCPL-063L will prevent transient voltage noise from the power hot swap circuit from disrupting the host controller side circuit.

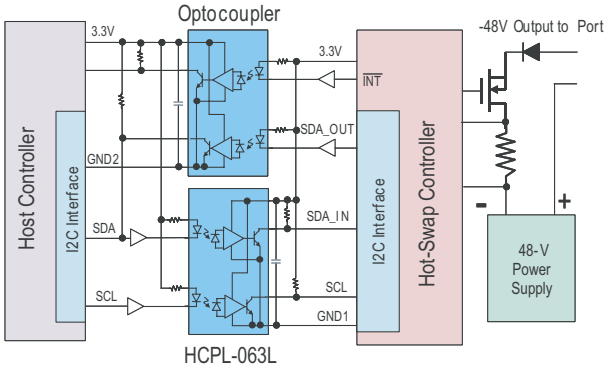

Figure 3. Optocoupler Isolated I2C Bus in PSE of a POE Switch

Analog-to-Digital Converter I2C Interface (Figure 4)

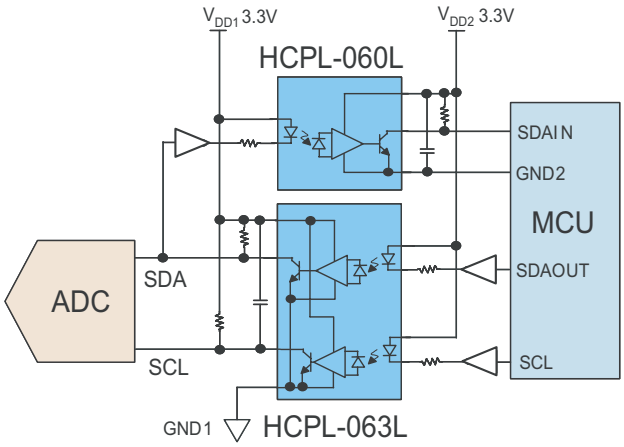

Figure 4. Optocoupler Isolated I2C Bus in A/D Conversion

Industrial and medical instruments may require optical isolation between mixed-signal and digital circuits. If a medical instrument sensor/probe is subjected to high voltage, safety electrical insulation is needed between the analog sensor and microcontroller/digital signal processor. Most isolation is intended to break any ground loop between the digital and analog circuitry because non-isolated grounds can result in high background noise in the system and affect A/D conversion accuracy.

The I2C bus provides a convenient interface between an A/D chip and microcontroller. A/D converters that incorporate an internal I2C interface are available on the market.

One dual-channel optocoupler, such as an HCPL-063L, can isolate the transmit clock and SDAOUT from the MCU/master to ADC/slave. One single channel optocoupler, such as an HCPL-060L, transmits SDAIN from the ADC/slave to MCU/master. An isolated DC/DC converter could derive power from the digital system to supply the A/D converter and VDD1- GND1 on the other side of two optocouplers.

Designing optical isolation for the I2C bus parallel clock and data signals requires consideration for optocoupler propagation delay and skew performance. Optocouplers with open-collector outputs are simple to directly connect to the I2C bus line. Optocouplers inherently feature high electromagnetic interference immunity through optical coupling and isolation boundary, which helps makes the equipment reliable and capable of meeting EMI standards.

AV02-2384EN - March 19, 2010