Design Considerations in Using the Inverter Gate Driver Optocouplers for Variable Speed Motor Drives

by Jamshed Namdar Khan

White Paper

Abstract

Inverter gate driver optocouplers are ideally suited for IGBT and MOSFET applications for variable speed motor drives. Their high output peak currents, coupled with high voltage safety standards certified galvanic insulation, very high common mode noise rejection isolation, solid state device level reliability, and very low power dissipation, make them indispensable inverter gate driver components. The design requirements and power dissipation considerations are discussed here to ensure that the appropriate gate driver optocouplers are selected to match the inverters' gate charge and power requirements.

UPS – Uninterruptible power supply

DTI – Distance through insulation

MTTF – Mean time to failure

VSD – Variable speed motor drives

UVLO – Under-voltage lockout protection

Introduction

Gate driver optocouplers are now commonly used for high power inverter (IGBT or MOSFET) applications such as: motor control, UPS, switching power supplies, high intensity lamp ballast, and induction heating. These inverter gate driver optocouplers have become a component of choice by design engineers because of the many fundamental and key advantages they provide over competing gate driver technologies. The advantages offered by these optocouplers include:

1. High voltage galvanic insulation (reinforced insulation levels) for safety and protection that includes either the one minute momentary withstand capability as certified through the UL1577, or the continuous working voltages as certified through IEC60747-5-2 optocoupler safety standards.

   These levels include up to 5000 Vrms/1 minute and 1414 Vpk (1000 Vrms or 1000 Vdc) working voltages, depending on the gate driver package selected.
2. Noise isolation: Ultra high common mode (dv/dt) noise rejection (CMR) at high common mode voltages (V_{CM})—up to 40 kV/µsec at V_{CM}=1500V is now available.
3. Physical spacing, such as creepage and clearance distances, mandated by safety standards. Some standards require an internal clearance which is also known as DTI.
4. Variable speed data rate capability from DC levels up to the maximum guaranteed speeds.
5. Very low detector power dissipation which helps in ease-of-design for providing isolated bootstrapped power supplies or switching power supplies.
6. Solid state reliability levels and very large MTTF.
7. Low input drive current or low input power requirements.
8. Small footprint area and package sizes (standard 300 mil DIPs), SO-16 or SO-8 packages. Dual gate driver optocouplers are also available.
9. Simplicity, ease-of-use, and very few external components are required.
10. Relatively low cost.

Analog optocouplers are also available for current sensing and fault detection, gate driver optocouplers for inverter gate driver applications, and digital optocouplers for digital data communications such as DeviceNet, Profibus, RS-485, RS-422, Rs-232, and Controller Area Network (CAN), etc.

The above advantages are the key reasons for using the gate driver optocouplers for VSD. The VSD ultimately translates into more efficient drives which result in significant power and cost savings. This is primarily due to the fact that the power consumed by a motor is proportional to the cube of its speed. If the speed of the motor is more carefully controlled to perform certain processes more efficiently, the result is significant energy savings over the life of operation. For this reason, the most popular market for VSD is consumer home appliances such as washing machines, refrigerators, air-conditioners, fans, mixers, and blenders.

This paper focuses on using the gate driver optocouplers for inverter applications in VSD. These same gate driver optocouplers can also be used in converter applications, such as boost or buck converters, switching power supplies, UPS applications, induction heating, and electric arc-welders, etc.

Dimensioning the Gate Driver Optocouplers for an IGBT or MOSFET

Figure 1 is a typical three phase induction motor (assumed to be in vector control mode). The six hex-bridge IGBT can be driven with a transformer gate drive, a discrete gate current amplifier drive, an integrated high voltage HVIC gate drive, or an optocoupler gate drive.

The primary emphasis here is optocoupler gate drivers for IGBT or MOSFET applications.

In selecting a particular inverter gate driver optocoupler, the questions that need to be addressed are:

- How much power is dissipated in the output of the gate driver?
- How much peak current does an IGBT require for proper switching characteristics?
- How much power is delivered to the IGBT gate?
- How does one determine what the IGBT gate charge Qg is?
- What gate resistor value to pick?
- How is the gate driver successfully dimensioned?

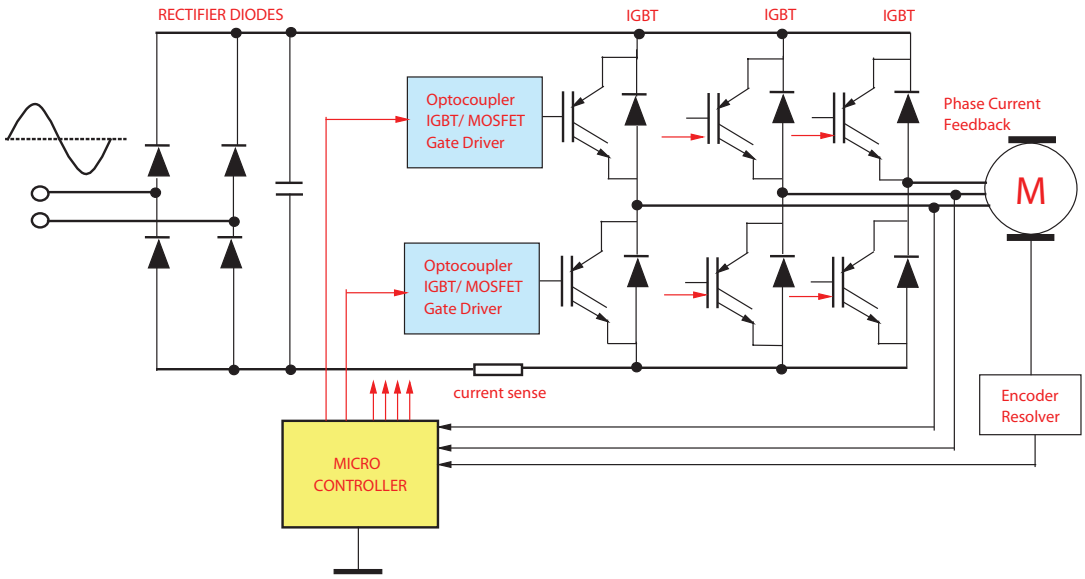

Figure 1. Three Phase Induction Motor with Optocoupler Gate Drivers

Figure 2 shows Avago Technologies' ACPL-3130 optocoupler gate driver configured with dual supplies, VCC and VEE. The negative supply VEE is used to provide a reverse gate-emitter voltage or negative gate voltage for a quicker or sharper turn-off of the IGBT when the output of the gate driver is in the low state.

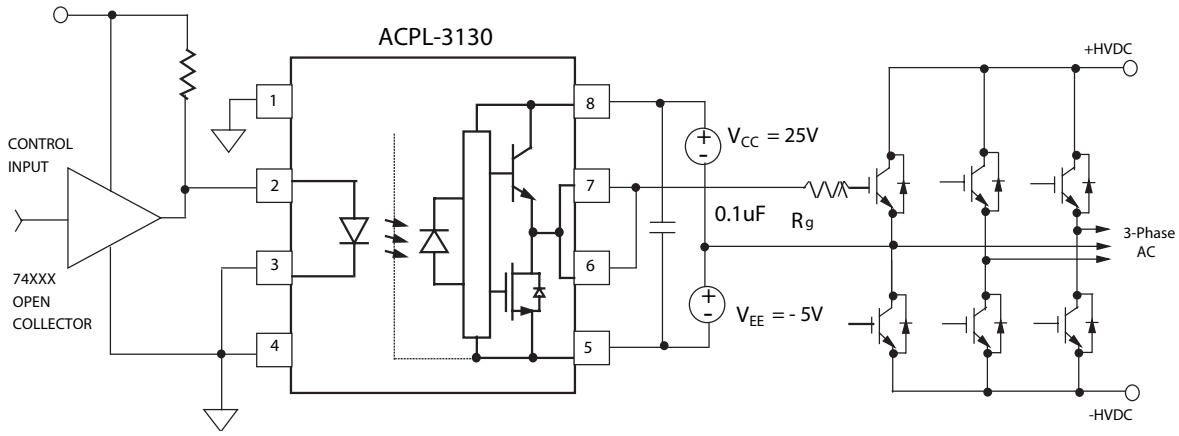

Figure 2. Optically Isolated Gate Driver Using the ACPL-3130 with Negative Gate Voltage (V_{EE}) for Faster IGBT Turn-OFF Requirements

1. How much total power is dissipated in the optocoupler gate driver? Use the following equation to find the answer.

   P_{TOTAL} (optocoupler) = $(D \times I_F \times V_F)+D \times Ibias(ON)\times(V_{CC}+V_{EE})+(1-D)\times Ibias(OFF) \times (V_{CC} + V_{EE})+ P_O(switching)$

   Where:

   D = duty cycle

   I_F = input drive current of the LED of the optocoupler

   V_F = LED forward voltage

   Ibias(ON) = is the quiescent supply ($V_{CC}+V_{EE}$) current in the output high state of the optocoupler (i.e. I_{CCH} parameter in the data sheet)

   Ibias(OFF) = is the quiescent supply ($V_{CC}+V_{EE}$) current in the output low state of the optocoupler, (i.e., I_{CCL} parameter in the data sheet)

   P_O (switching) = is the power dissipated in the output pin of the optocoupler and is a function of the switching frequency and energy (E) supplied to the gate of the IGBT

   P_{TOTAL}(optocoupler) = Power dissipated in the optocoupler

2. Is the output frequency (f_{SW}) dependent output power P_O(switching) dissipated in the output pin of the optocoupler?

   $P_O(switching) = E(switching)\times f_{SW}(switching)$

   Since the energy stored in the gate capacitance of the IGBT is also the energy supplied by the output of the optocoupler to the IGBT gate capacitance:

   $E(switching) = ½(CV^2)$

   Where:

   C = gate capacitance of the IGBT

   V = output high voltage of the optocoupler gate driver. Is proportional to the power supply voltage, in this case: ($V_{CC} + V_{EE}$)

   When the output of the optocoupler is in the high state (Voh), it can be shown that the energy supplied by the gate driver optocoupler to the IGBT is:

   $E(switching)=½[(QgV_{CC}) + CgeV_{EE}^2]$

   When the gate driver output is high, the power delivered to the gate of the IGBT from Equation 2 is:

   $Po(Voh)=PO(switching)=E(switching)\times f_{SW}(switching) = E\times f_{sw}=(f_{sw}/2)\times[(QgV_{CC})+CgeV_{EE}^2]$

   When the output of the gate driver optocoupler is in the low state, an equal amount of energy must be removed from the gate (conservation of energy principle):

   $Po(vol)=Po(switching)= (f_{sw}/2)\times[(QgV_{CC})+CgeV_{EE}^2]$

3. How much of this power is dissipated in the optocoupler output?

   The output resistance R(on) of the optocoupler is in series with the Rg(ext) and Rg(int) of the IGBT. Most high performance Avago Technologies' gate driver optocouplers have bipolar triple Darlington pull-up stage, and MOSFET output pull-down stage.

   For the MOS Pull-down output stage, when the gate driver is sinking the current:

   $Po(vol)= [Ron(vol) / (Ron(vol)+Rg(ext)+Rg(int))]\times(fsw/2)\times[(QgV_{CC})+CgeV_{EE}^2]$

   For the triple darlington pull-up stage, when the driver is sourcing current:

   $Po(voh)=[Ron(voh) / (Ron(voh)+Rg(ext)+Rg(int))]\times(fsw/2)\times[(QgV_{CC})+CgeV_{EE}^2]$

   Considering the duty cycle, the switching power dissipation in the output of the gate driver optocoupler as P(sw):

   $Po(vol)=(1-D)\times[Ron(vol) / (Ron(vol)+Rg(ext)+Rg(int))]\times(f\ sw/2)\times[(QgV_{CC})+CgeV_{EE}^2]$

   $Po(voh)=D \times [Ron(voh) / (Ron(voh)+Rg(ext)+Rg(int))]\times(f\ sw/2)\times[(QgV_{CC})+CgeV_{EE}^2]$

   Where:

   Ron(vol) = output resistance of the optocoupler in the output low state

   Ron(voh) = output resistance of the optocoupler in the output high state

   Rg(ext) = the external gate resistor at the output of the optocoupler to limit the peak current to the gate of IGBT

   Rg(int) = the internal gate resistance of the IGBT

   D = duty cycle between (0 to 1)

   Qg = total gate charge of the IGBT at the specified gate voltage

   fsw=switching frequency

   If we assume that the Rg(int) of the IGBT can be neglected, and Ron(vol) is approximately equal to Ron(voh), then the power dissipation formulas can be simplified as:

   $Po(switching)=Pon(vol)+Pon(voh)=[Ron / (Ron+Rg(ext)]\times(fsw)\times[(QgV_{CC})+CgeV_{EE}^2]$

   A good approximation for the Ron(oh) and Ron(ol) of Avago Technologies' triple Darlington output-high and MOSFET output-low stage gate driver optocouplers is approximately 1.5ohms. The total power dissipated in the optocoupler package is:

   P_{total} (optocoupler)$=(D\times I_F\times V_F)+D\times Ibias(ON)\times(V_{CC}+V_{EE})+ (1-D)\times(Ibias(OFF)\times(V_{CC}+V_{EE})+P_O(switching)$

   Where Po(switching) is now identified:

   $Po(switching)=Pon(vol)+Pon(voh)=[Ron/(Ron+Rg(ext)]\times(fsw)\times[(QgV_{CC})+CgeV_{EE}^2]$

4. Sometimes, it is useful to calculate energy supplied to the output of the optocoupler per cycle, which is defined as:

   $Po(switching)/fsw =(Pon(ol)+Pon(oh)\ ) / fsw=[Ron(oh) / (Ron(oh)+Rg(ext)\times[(QgVCC)+CgeV_{EE}^2\ ]$

5. The output peak current supplied to the gate of the IGBT by the gate driver optocoupler is:

   $I_{OH}(peak)=[V_{OH} - V_{EE}\ ] / Rg(ext)$

   Where $V_{OH} = V_{CC} - 2V$ (2V is typical output high saturation voltage and V_{EE} is the negative gate voltage, typically proportioned at $V_{EE} = -5V$)

6. The turn-ON time, td(on) of the IGBT can be calculated as:

   td(on) =Qg / Ipeak

   Where Qg is the total gate charge that can be picked readily from the IGBT data sheets, as depicted in the gate voltage vs. gate charge shown in Figure 3.

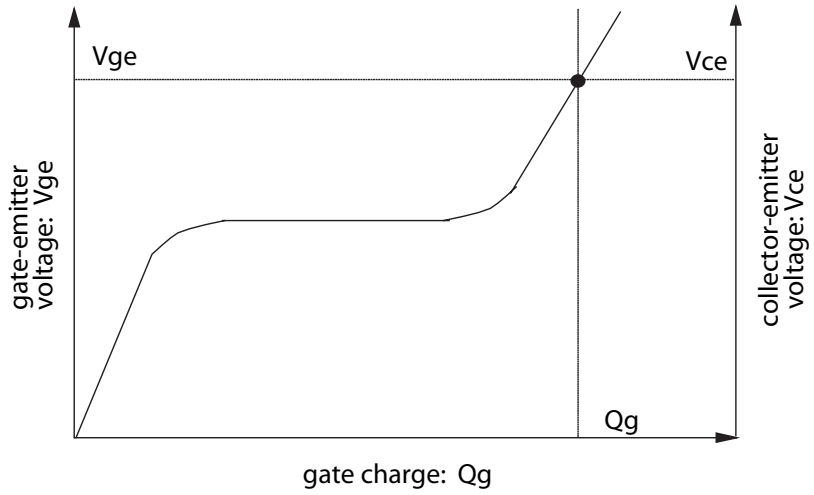

Figure 3. IGBT Vge (gate-emitter) Voltage vs. Gate Charge (Qg) Curves

Short Circuit Current Faults and IGBT De-Saturation Detection

Avago Technologies' high performance gate driver optocouplers, such as the HCPL-316J, ACPL-332J, and ACPL-331J, provide critical safety functions, e.g., de-saturation fault detection and under-voltage lockout protection (UVLO). The de-saturation fault detection circuit provides protection for the power semiconductor switches against short circuit current events which may lead to the destruction of these power switches. These short circuit current faults can usually be attributed to phase current and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise, computational errors, or overload conditions.

The IGBT collector-emitter voltage, VCESAT, is monitored by the DESAT pin of the gate driver optocoupler (pins 14 and 16 of Figure 4).

When there is a short circuit in an application, and a high current flows through an IGBT, the IGBT will go out of saturation mode and its V_{CESAT} voltage will increase. A fault is detected by the optocoupler gate driver (while the IGBT is ON) once this V_{CESAT} voltage goes above the internal de-saturation fault detection threshold voltage (which is typically 6.5V for the ACPL-332J). The DESAT detection circuit is disabled when the gate driver optocoupler output voltage is in the low state. This fault detection triggers two events:

1. Output (Vout) of the optocoupler gate driver is slowly brought low in order to "softly" turn off the IGBT and prevent large di/dt induced voltage spikes.
2. An internal optically isolated feedback channel is activated, which brings the Fault output low for the purpose of notifying the microcontroller of the fault condition. At this point, the microcontroller must take appropriate action to shutdown or reset the motor drive.

The DESAT fault detection circuitry should remain disabled for a short time following the turn-on of the IGBT to allow the collector voltage V_{CE} to fall below the DESAT threshold. The time period, called the DESAT blanking time, ensures that there is no nuisance fault tripping during the IGBT turn-on. This time also represents the time it takes for the driver to go to a fault condition. The blanking time is controlled by the internal DESAT current source, I_{CHG} of 250µA (typical), the DESAT threshold voltage, V_{DESAT} (6.5V typical), and the external blank capacitor, C_{BLANK}.

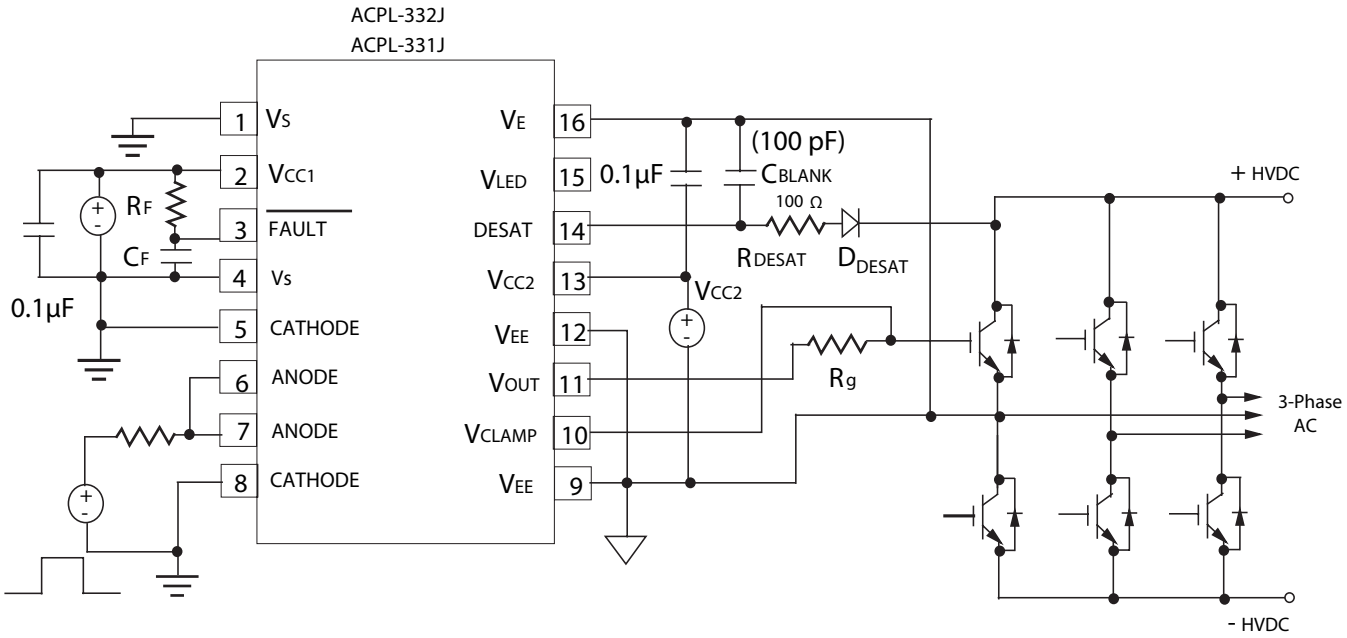

Figure 4. Recommended Application Circuit with Desaturation Detection Using ACPL-332J or ACPL-331J Gate Driver Optocouplers

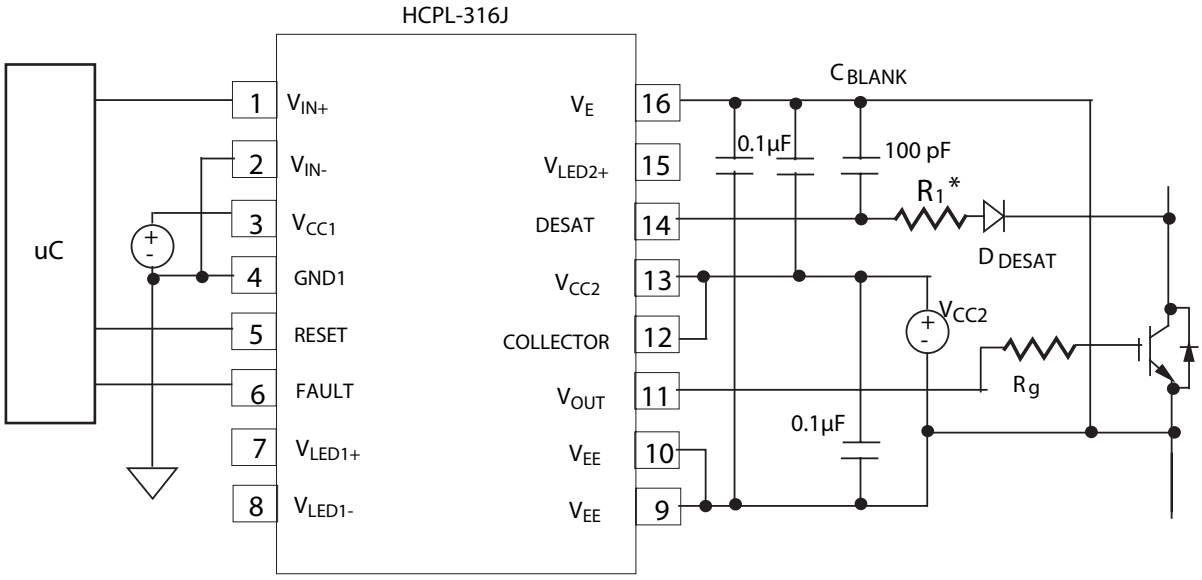

Figure 5. Desaturation Fault Detection Circuit Using the HCPL-316J

The blanking time is determined by:

$I_C = C \times (\Delta V / \Delta T)$

$t_{BLANK} = (C_{BLANK} \times V_{DESAT}) / I_{CHG}$

The recommended value for the C_{BLANK} is 100 pF which gives a blanking time (t_{BLANK}) of 2.7µs (Condition I_{CHG} = 240µA (typical), V_{DESAT} = 6.5V (typical); page 8 of ACPL-332J datasheet AV02-0120EN-May 7, 2007).

The DESAT detection threshold voltage of 6.5V (typical) can be reduced by placing a string of DESAT diodes in series or by placing a low voltage zener diode in series.

For the string of DESAT diode method:

$V_{DESAT\ (NEW\ THRESOLD)} = (6.5 - n \times V_F)$

For the DESAT diode with the Zener Diode method:

$V_{DESAT\ (NEW\ THRESOLD)} = (6.5 - V_F - V_Z)$

Where n is the number of DESAT diodes, V_Z is the zener voltage value, and V_F is the forward voltage of the DESAT diode. This allows a designer to conveniently select an appropriate DESAT detection threshold voltage.

Note the "blanking capacitor charging current" parameter (page 9 of the data sheet for the HCPL-316J optocoupler gate driver) indicated in Table 1.

Table 1. Blanking Capacitor Charging Current for the HCPL-316J Gate Driver

Blanking Capacitor Charging Current, ICHG	**Minimum**	**Typical**	**Maximum**	**Units**
	130	250	330	µA

Calculate the blanking time based on the blanking capacitor charging current as shown in Table 1 for the HCPL-316J gate driver optocoupler using the equations below.

$I_{CHG} = C \times (\Delta V / \Delta t)$

Transposing and calculating for the blanking time, Δt, with the internal typical de-saturation voltage detection level of 7V (for the HCPL-316J or the HCPL-332J) we find:

Δt (maximum)=(100 pF×7V) / 130µA=5.38µsec

Δt (typical)=(100 pF×7V) / 250µA=2.80µsec

Δt (minimum)=(100 pF×7V) / 330µA=2.12µsec

For most applications the above indicated blanking time variation would be acceptable. To minimize the blanking time variation, an external blanking circuit approach is shown in Figure 6.

Figure 6 shows a concept for an external blanking circuit. This method uses one additional external resistor, RB, connected from the output to the DESAT pin 14 of the HCPL-316J gate driver. This allows an additional blanking capacitor charging current component from the output of the gate driver optocoupler through RB, and this adds to the internal current source of the gate driver optocoupler. This higher external blanking capacitor charging current allows a designer greater flexibility in choosing both an appropriate value of the blanking capacitor, C_B, and an appropriate current through the choice of the external resistor R_B. By adjusting the capacitance of the blanking capacitor C_B and the additional external blanking current through R_B, a designer can set a precise blanking time.

The voltage on the blanking capacitor can be written as:

$V_C(t)=V_I - V_f\,[1-e^{(-t/RC)}]$

Where:

V_{EE} = -9V

V_{CC2} = 17V

R_B = 1000 kΩ

C_B = 4700 pF (blanking capacitor)

At t =0

$V_C(0) = VI$ = -9V

At t = ∞

$V_C(\infty) = VI + Vf$ = -9V + 26V = 17V

This can be written as:

$V_C(t)=7V$= -9V + 26[1– $e^{(-t/RC)}$]

or $e^{(-t/RC)}$ =[1 – 16/26]

($-t_{blank}$ /RC)=ln (0.3846)

Calculating for the blanking time, t(blank), with R_B = 1000Ω and C_B = 4700pF:

t(blank)= - R_BC_B ln(0.3846)=4.5µsec

This external blanking time (t_{blank}) calculation shows that by introducing an additional external blanking capacitor charging current (I_{CHG}) through a resistor R_B, there is greater control over the blanking time. Figure 7 shows the fault detection and rest timing waveforms of the HCPL-316J gate driver optocoupler.

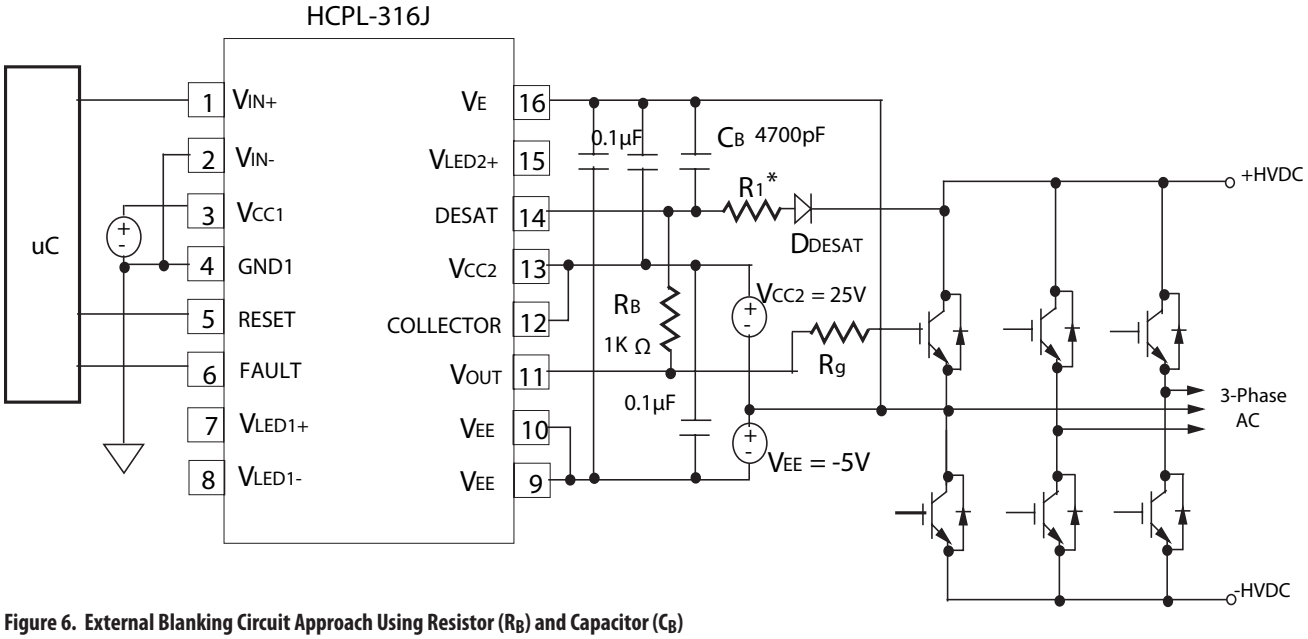

Figure 6. External Blanking Circuit Approach Using Resistor (R_B) and Capacitor (C_B)

Discharging the IGBT gate through Negative Gate Bias or Active Miller Clamp

Unlike a MOSFET, an IGBT normally requires a negative gate voltage to minimize the switching losses due to the slow "turn-off tail current". The negative gate voltage helps to quickly reverse bias of the gate-emitter voltage during the turn-OFF and minimize the switching losses. An additional benefit of the negative gate bias voltage is an improvement in the dv/dt noise immunity of the IGBT. The gate-to-collector "Miller capacitance" can induce a false turn-ON due to high collector-to-emitter dv/dt induced during the switching sequence. Most Avago Technologies' gate driver optocouplers (such as the HCPL-316J, HCPL-3130, and HCPL-3120) can be operated either with a single supply or with dual supplies if a negative gate drive is desired for a quick turn-OFF of the IGBT as shown in Figures 2 and 6.

To avoid the necessity of a dual power supply to provide the "negative gate drive" for a fast turn-off of the IGBT, another method employed by some Avago Technologies' gate drivers is to provide an alternative low impedance path with a high sink current capability called an Active Miller clamp, available in gate drivers such as the ACPL-332J and the ACPL-331J). Figure 8 is the ACPL-332J internal block diagram, showing the additional power FET transistor that provides the shunt low impedance path for gate discharge, and also clamps the gate of the IGBT at a low voltage during the entire turn-OFF time.

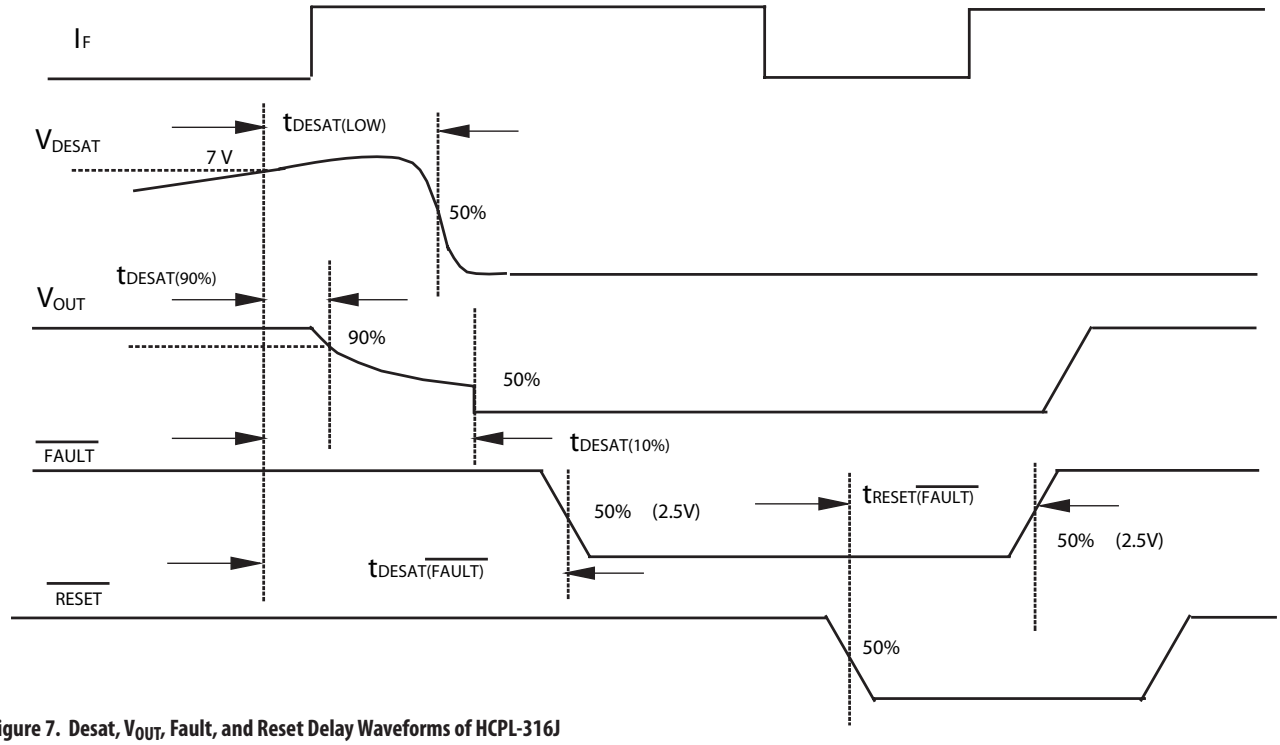

Figure 7. Desat, V_{OUT}, Fault, and Reset Delay Waveforms of HCPL-316J

Pin (10) of the ACPL-332J and ACPL-331J is the Active Miller clamp pin. An internal high power MOSFET transistor offers the low impedance path for the gate turn-off and discharge current. This "switch" shorts the gate-emitter voltage of the IGBT after the threshold level is reached. The currents associated with the Miller capacitance are also shunted by this switch instead of flowing through the output (Vout) of the gate driver optocoupler (Pin 11).

During the turn-OFF, the gate voltage of the IGBT is monitored and clamp output is activated when the gate voltage goes below 2V (relative to V_{EE}, pins 9 and 12). The clamp voltage is typically V_{OL}+ 2.5V for a Miller current up to 1.1A. The Active Miller clamp function is disabled when the LED input is triggered again, and the output of the gate driver optocoupler is in the output high state.

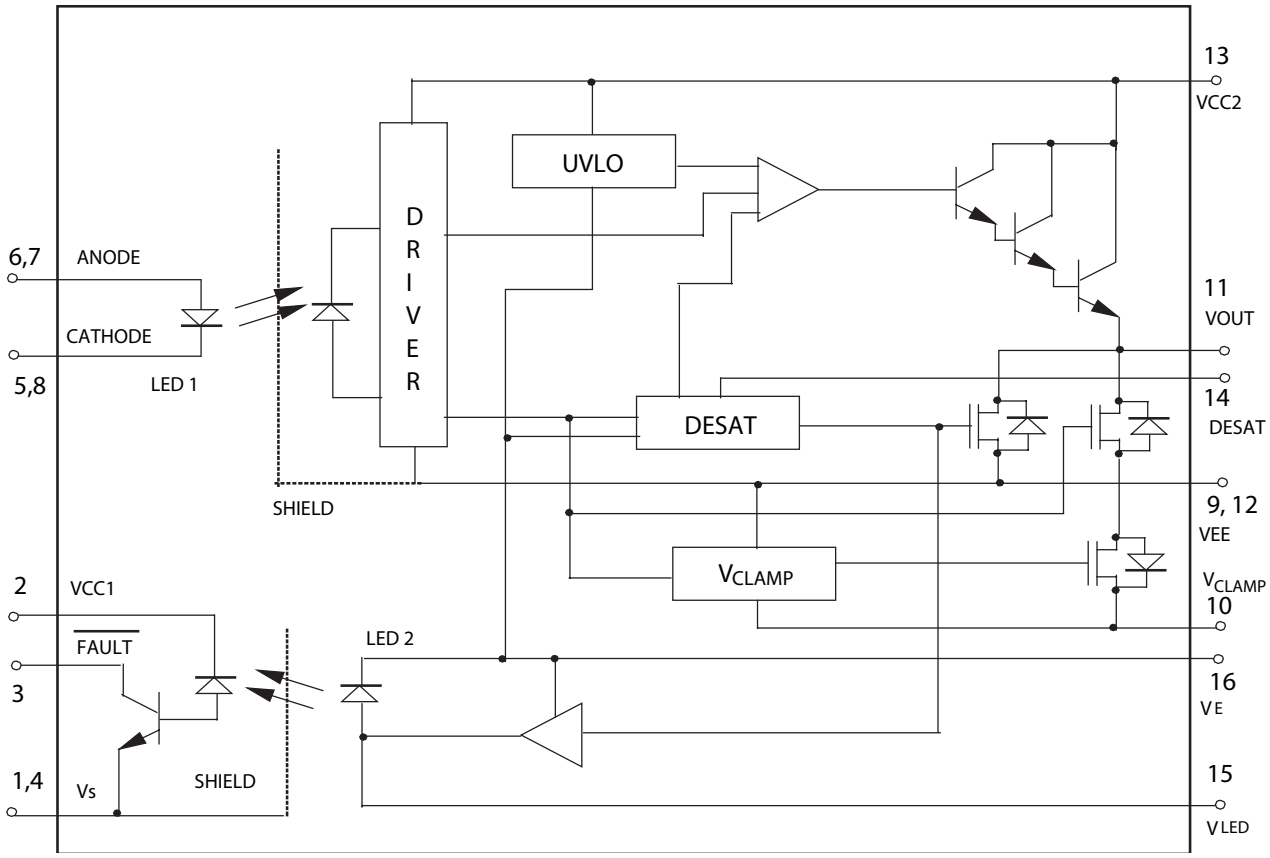

Figure 8. ACPL-332J Block Diagram, with Active Miller Clamp for Fast Gate Turn-OFF of an IGBT or MOSFET(Pin 10)

Conclusion

In this paper we have considered the inverter gate driver optocoupler for variable speed three phase induction motors. Gate driver optocouplers provide some key and fundamental features that are required for high power bus applications using IGBTs or MOSFETs. These features include high insulation voltages for galvanic safety isolation, high output peak currents, and ultra-high dv/dt common mode noise immunity (CMR). Safety features include de-saturation fault detection, under-voltage lockout, optically isolated fault-status feedback for the micro-controller, and soft output turn-off to prevent high di/dt induced voltage spikes. To minimize the IGBT switching power losses, these gate driver optocouplers also provide the capability for a negative gate bias voltage through the use of dual power supplies. Other gate drivers provide Active Miller clamps which preclude the need for the negative gate supply voltage.

Dynamic maximum power dissipation equations were derived for the gate driver optocoupler as a function of the gate resistor, power supply levels, and switching frequency.

References

[1] Muhammad H. Rashid, Editor, " Power Electronics Handbook," 2nd Edition, Academic Press, San-Diego, 2007.

[2] Muhammad H. Rashid, "Power Electronics: Circuits, Devices, and Applications," 2nd Edition, Prentice-Hall, New Jersey, 1993.

[3] Jamshed Namdar Khan, "Optocouplers for Variable Speed Motor Control Electronics in Consumer Home Appliances," Proceedings of the 52nd International Appliance Technical Conference (IATC), pp. 256-285, 2001.

[4] Jamshed Namdar Khan, "Using Hermetic Optocouplers in Military and Space Electronics," 5th Annual International Conference, Commercialization of Military and Space Electronics, 2001.

[5] Jamshed Namdar Khan, "Regulatory Guide to Isolation Circuits," Hewlett-Packard publication number 5965-5853E, January 1, 1997, and Avago Technologies Publication Number 5989-2937EN, July 17, 2007.

[6] Malcolm Barnes, "Practical Variable Speed Drives and Power Electronics," Newnes, Oxford, 2003.

[7] "Desaturation Fault Detection," AN 5324, Avago Technologies, 2007.

[8] "Soft Turn-Off Feature," AN 5315, Avago Technologies, 2007.

[9] " Active Miller Clamp," AN 5314, Avago Technologies, 2007.

[10] Yeo Siok Been, Jamshed Namdar Khan, and Derek Chng Peng Hui, "Designing Medical Devices for Isolation and Safety," EDN (Electronic Design, Strategy, News), pp. 75-78, May 24, 2007.

This paper was first presented at the Power Electronics Technology Conference 2007.

AV02-0803EN - March 6, 2010